

Claims

We claim:

- 1 1. A switching regulator, comprising:
 - 2 a driver coupled to receive a first high side reference voltage;
 - 3 an input switching device having a source node, a drain node, and a
 - 4 control node, the control node coupled to an output of the driver, the drain
 - 5 node coupled to receive an input voltage;
 - 6 a diode coupled between the source node of the input switching device
 - 7 and ground;
 - 8 an inductor having a first end coupled to the source node of the input
 - 9 switching device;
 - 10 a first output switching device having a drain node coupled to the
 - 11 second end of the inductor, the first output switching device having a control
 - 12 node coupled to a high side output;
 - 13 a second output switching device having a drain node coupled to the
 - 14 second end of the inductor, the first output switching device having a control
 - 15 node coupled to a low side output;
 - 16 an output load coupled to the source nodes of the first and second
 - 17 output switching devices; and
 - 18 a low power control circuit coupled across the inductor, wherein the
 - 19 low power control circuit monitors the current across the output load and
 - 20 automatically initiates the low power mode of the switching regulator
 - 21 independent of the value of the output load and the input voltage.
- 1 2. A switching regulator as recited in claim 1, wherein the low power control
- 2 circuit comprises:
 - 3 a low power switching device having a control node coupled to the
 - 4 high side output and a drain node coupled to the second end of the inductor;

5 an amplifier coupled to the source node of the low power switching
6 device and the first output switching device;

7 a first current mirror coupled to the amplifier to mirror the difference
8 between the output current through the output load and the current supplied
9 at the second end of the inductor;

10 a second current mirror coupled to the first current mirror;

11 a current source coupled to the second current mirror;

12 a capacitor coupled across the current source;

13 a comparator coupled to the second current mirror and coupled to
14 receive a predetermined voltage source to compare the voltage across the
15 capacitor with the predetermined voltage source;

16 a first AND gate coupled to the comparator and to receive the low
17 power mode signal;

18 a second AND gate coupled to the comparator and to receive the low
19 power mode signal and the inductive switch signal;

20 a first counter coupled to the first AND gate to provide a low power
21 entry signal; and

22 a second counter coupled to the second AND gate to provide a low
23 power exit signal.

1 3. The switching regulator as recited in claim 1, wherein the first input
2 switching device is a transistor.

1 4. The switching regulator as recited in claim 1, wherein the second input
2 switching device is a transistor.

1 5. The switching regulator as recited in claim 1, wherein the first output
2 switching device is a transistor.

1 6. The switching regulator as recited in claim 1, wherein the second output
2 switching device is a transistor.

1 7. The switching regulator as recited in claim 1, wherein the first input
2 switching device is a metal-oxide-semiconductor field-effect transistor (Mos
3 FET).

1 8. The switching regulator as recited in claim 1, wherein the second input
2 switching device is a Mos FET transistor.

1 9. The switching regulator as recited in claim 1, wherein the first output
2 switching device is a Mos FET transistor.

1 10. The switching regulator as recited in claim 1, wherein the second output
2 switching device is a Mos FET transistor.

1 11. The switching regulator as recited in claim 1, wherein the output load
2 comprises:
3 a capacitor; and
4 a resistor coupled in parallel with the capacitor.

1 12. The switching regulator as recited in claim 2, wherein the low power
2 switching device is a transistor.

1 13. The switching regulator as recited in claim 2, wherein the low power
2 switching device is a sense FET transistor.

1 14. The switching regulator as recited in claim 2, wherein the first current
2 mirror, comprises:
3 a first transistor, having a drain node coupled to the source node of the
4 low power switching device; and

5 a second transistor coupled to the first transistor, the control node of
6 the first and second transistors couple to the amplifier, the source node of the
7 second transistor coupled to the source node of the first transistor.

1 13. The switching regulator as recited in claim 2, wherein the second current
2 mirror, comprises:

3 a first transistor, having a drain node, a source node, and a control
4 node, the drain node coupled to the control node and the drain node coupled
5 to the first current mirror; and

6 a second transistor having a drain node, a control node and a source
7 node, the control node coupled to the control node of the first transistor, the
8 source node coupled to the source node of the first transistor, the drain node
9 coupled to the capacitor.

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